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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,426	12/07/2001	Daniel M. Castagnozzi	applied_114	9539

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,426	CASTAGNOZZI ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/07/2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, claims 17-32 in the reply filed on 07/06/2004 is acknowledged.

Oath/Declaration

2. In view of the new Declaration filed 04/19/2004, the Examiner withdraws any objection to the Declaration.

Drawings

3. The proposed drawing correction filed 04/19/2004 is approved.

The drawings are objected to because of illegible handwriting in the drawings. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Response to Arguments

4. Applicant's arguments with respect to claim 17-48 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 17-48 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claim 17 recites, "the causal circuit comparing a current bit estimate to bit value decisions made across a plurality of clock cycles, the causal circuit having an output to supply a bit value for the current bit estimate determined in response to the causal bit value comparisons". The omitted structural cooperative relationships are: the relationship between "a current bit estimate", "bit value decisions" and "causal bit value comparisons". It is not clear how a current bit estimate" and "bit value decisions" relate to "causal bit value comparisons". It is not clear how "a bit value for the current bit estimate" relates to "the current bit estimate", that is, is the "bit value" a modified current bit estimate or is it the same bit value as the original current bit estimate?
Claims 33 and 35 recite similar language as in claim 17.

Claims 17-48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 17 recites, "comparing a current bit estimate to bit value decisions made across a plurality of clock cycles". It is not clear whether the Applicant intends 1) – a comparison made across a plurality of clock cycles between a current bit estimate and bit value decisions -- or 2) --using bit value decisions made across a plurality of clock cycles in a comparison between a current bit estimate--.
In addition, a current bit estimate is the current estimate at a particular clock cycle; it does not make sense to claim a current bit estimate across a plurality of clock cycles since the current bit estimate for the first cycle is not the current bit estimate for the second cycle. What is being compared, the current bit estimate for the first cycle or current bit estimates for each cycle?

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 17, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andresen; Rolf et al. (US 3670304 A) in view of Abe; Katsuaki et al. (US 5781588 A, hereafter referred to as Owaki).

35 U.S.C. 103(a) rejection of claims 17 and 33.

Andresen teaches a multi-threshold decision circuit having an input to accept a data stream encoded with forward error correction FEC (Amplitude Sense and Data Gates 20 in Figures 1 & 3 in Andresen are a multi-threshold decision circuit having an input to accept a data stream encoded with forward error correction FEC), an input to accept threshold values (Input Line 44 in Figure 1 of Andresen provides a Change Threshold value to Amplitude Sense and Data Gates 20), and outputs to provide bit estimates responsive to a plurality of voltage threshold levels (Output Lines 27 and 72 in Figures 1 & 3 of Andresen provide bit estimates responsive to a plurality of voltage threshold levels); a non-casual circuit having inputs to accept bit estimates from the multi-threshold decision circuit (Data/Error Detectors in Figures 1 & 3 of Andresen are a non-causal circuit having inputs to accept bit estimates from the Amplitude Sense and Data Gates multi-threshold decision circuit 20), the non-casual circuit comparing a current bit estimate to bit value decisions made across a plurality of clock cycles (non-casual circuit Data/Error Detectors in Figures 1 & 3 of Andresen comprise Data Detector 28 in Figure 1 & 6 comprising Comparators 124 & 138 in Figure 6 for

comparing a current bit estimate D in Figures 6 & 7 to bit value reference decisions R1 and R2 made across a plurality of clock cycles; Note: bit value reference decisions R1 and R2 are predetermined reference values made across a plurality of clock cycles); the non-casual circuit having an output to supply a bit value for the current bit estimate determined in response to the non-casual bit value comparisons (Data Detector 28 inside the non-casual circuit Data/Error Detectors 24 in Figures 1 & 3 of Andresen supplies a Data output which is the current bit estimate determined in response to the non-casual bit value comparisons); a forward error correction FEC circuit having an input to receive the first bit value from the non-casual circuit (Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen are an FEC circuit having an input to receive a first bit value from the non-casual circuit Data/Error Detectors 24), the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding (the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen decode and correct the incoming data stream), the FEC circuit having an output to supply a stream of corrected data bits (the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen have an output to supply the Read Data stream of corrected data bits); and, a statistics circuit having an input to accept the first bit value from the non-casual circuit, an input to accept the stream of corrected data bits from the FEC circuit, and an output to supply threshold values to the multi-threshold circuit in response to analysis of the FEC error statistics (Check Change Threshold Circuits 26, 90 and 92 in Figures 1 & 3 of Andresen are a statistics circuit having an input to accept the first bit value from the non-casual circuit

Data/Error Detectors 24, an input to accept the stream of corrected data bits from the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96, and an output to supply threshold values to the multi-threshold circuit Amplitude Sense and Data Gates 20 in Figures 1 & 3 in response to analysis of the FEC error statistics).

However Andresen does not explicitly teach the specific use of non-return to zero NRZ. Abe, in an analogous art, teaches use of non-return to zero NRZ (see Col. 23, lines 42-46, Abe). Note: the circuit in Andresen is designed to resolve and reproduce digital data and NRZ encoded data is digital data; hence it would be obvious to apply the teachings in the Andresen patent to a specific type of data for which it was designated such as NRZ which is a widely used form of encoding for magnetic storage devices.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Andresen with the teachings of Abe by including use of non-return to zero NRZ. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of non-return to zero NRZ would have provided the opportunity to apply the teachings in the Andresen patent to a specific type of data for which it was designated such as NRZ which is a widely used form of encoding for magnetic storage devices in order to equalize BER's for respective different symbol states (col. 36, lines 27-29 in Abe).

35 U.S.C. 103(a) rejection of claim 35.

Andresen teaches a multi-threshold decision circuit having an input to accept a data

stream encoded with forward error correction FEC (Amplitude Sense and Data Gates 20 in Figures 1 & 3 in Andresen are a multi-threshold decision circuit having an input to accept a data stream encoded with forward error correction FEC), an input to accept threshold values (Input Line 44 in Figure 1 of Andresen provides a Change Threshold value to Amplitude Sense and Data Gates 20), and outputs to provide bit estimates responsive to a plurality of voltage threshold levels (Output Lines 27 and 72 in Figures 1 & 3 of Andresen provide bit estimates responsive to a plurality of voltage threshold levels); a non-casual circuit having inputs to accept bit estimates from the multi-threshold decision circuit (Data/Error Detectors in Figures 1 & 3 of Andresen are a non-causal circuit having inputs to accept bit estimates from the Amplitude Sense and Data Gates multi-threshold decision circuit 20), the non-casual circuit comparing a current bit estimate to bit value decisions made across a plurality of clock cycles (non-casual circuit Data/Error Detectors in Figures 1 & 3 of Andresen comprise Data Detector 28 in Figure 1 & 6 comprising Comparators 124 & 138 in Figure 6 for comparing a current bit estimate D in Figures 6 & 7 to bit value reference decisions R1 and R2 made across a plurality of clock cycles; Note: bit value reference decisions R1 and R2 are predetermined reference values made across a plurality of clock cycles); the non-casual circuit having an output to supply a bit value for the current bit estimate determined in response to the non-casual bit value comparisons (Data Detector 28 inside the non-casual circuit Data/Error Detectors 24 in Figures 1 & 3 of Andresen supplies a Data output which is the current bit estimate determined in response to the non-casual bit value comparisons); a forward error correction FEC circuit having an

input to receive the first bit value from the non-casual circuit (Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen are an FEC circuit having an input to receive a first bit value from the non-casual circuit Data/Error Detectors 24), the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding (the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen decode and correct the incoming data stream), the FEC circuit having an output to supply a stream of corrected data bits (the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen have an output to supply the Read Data stream of corrected data bits); and, a statistics circuit having an input to accept the first bit value from the non-casual circuit, an input to accept the stream of corrected data bits from the FEC circuit, and an output to supply threshold values to the multi-threshold circuit in response to analysis of the FEC error statistics (Check Change Threshold Circuits 26, 90 and 92 in Figures 1 & 3 of Andresen are a statistics circuit having an input to accept the first bit value from the non-casual circuit Data/Error Detectors 24, an input to accept the stream of corrected data bits from the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96, and an output to supply threshold values to the multi-threshold circuit Amplitude Sense and Data Gates 20 in Figures 1 & 3 in response to analysis of the FEC error statistics).

However Andresen does not explicitly teach the specific use of non-return to zero NRZ or the use of FEC error statistics to set the threshold.

Abe, in an analogous art, teaches use of non-return to zero NRZ (see Col. 23, lines 42-46, Abe). Note: the circuit in Andresen is designed to resolve and reproduce digital data

and NRZ encoded data is digital data; hence it would be obvious to apply the teachings in the Andresen patent to a specific type of data for which it was designated such as NRZ which is a widely used form of encoding for magnetic storage devices. Figure 37 of Abe teaches BER CALC circuit for producing error statistics for use in threshold adjusting circuit 2604. Note: Abe teaches that Figure 37 is a modification of Figure 33 in Abe using BER in order to equalize BER's for respective different symbol states (col. 36, lines 27-29 in Abe).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Andresen with the teachings of Abe by including use of non-return to zero NRZ. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of non-return to zero NRZ would have provided the opportunity to apply the teachings in the Andresen patent to a specific type of data for which it was designated such as NRZ which is a widely used form of encoding for magnetic storage devices in order to equalize BER's for respective different symbol states (col. 36, lines 27-29 in Abe).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 17-48 are provisionally rejected under the judicially created doctrine of double patenting over claims 16-28 of copending Application No. 10/077,332. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: the claims language of claims 1-48 in the current application is substantially embedded in claims 16-28 of copending Application No. 10/077,332.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sugiyama; Tokuji (US 5057946 A) teaches a magnetic disk drive

apparatus which provides an improved reliability in reading out data from magnetic disks.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2133